



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,567	03/31/2004	Nigel C. Paver	MP1534	9397
68933	7590	09/10/2007	EXAMINER	
MARVELL/FINNEGAN HENDERSON LLP c/o FINNEGAN, HENDERSON, FARABOW, GARNETT et. al. 901 NEW YORK AVENUE WASHINGTON, DC 20001-4413			CRIBBS, MALCOLM D	
		ART UNIT	PAPER NUMBER	
		2115		
		MAIL DATE	DELIVERY MODE	
		09/10/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/815,567	PAVER, NIGEL C.
	Examiner	Art Unit
	Malcolm D. Cribbs	2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 19 June 2007.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-23 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-23 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____. 	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Claims 1-23 are presented for examination.

5

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10 Claims 9, and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

15 Claim 9 uses the phrase "capable of" which constitutes a use limitation and thus renders the claims indefinite as to what structure is embraced by the metes and bounds of the claim language. See MPEP § 2111.04.

20 Claim 14 uses the phrase "capable of" which constitutes a use limitation and thus renders the claims indefinite as to what structure is embraced by the metes and bounds of the claim language. See MPEP § 2111.04.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

5

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Rotem [Publication No. US 2004/0128663] in view of Boutaghou et al [Patent No. US

5,732,215].

10

As per claims 1, and 14, Rotem teaches the invention comprising:

circuitry on a first node, the circuitry connected to the chip:

monitoring one or more parts of the application by a sensor attached to the chip [Page 2, paragraph 0018; wherein parts of the application [certain threads] running on the chip [core] are monitored while recording the thermal activity; wherein a process is made up of multiple threads wherein Rotem teaches monitoring a certain thread, thus a part of the process, a part of an application];

for at least one of the parts of the application, correlating the event data with the parts of the application [Page 2, paragraph 0018; wherein Rotem correlates the thermal activity recorded with that certain thread in order to control the thread allocation]; and

a performance analyzer [thread allocation unit] on a second node, the performance analyzer communicatively coupled to the circuitry on the first node to use the correlated information [0021].

25

Rotem discloses a method of detecting temperature of a chip above a threshold while running certain applications, thus eliminating high temperature situations.

Although Rotem teaches recording the history of high power usage in a thermally significant period of time [Page 2, paragraph 0018], Rotem does not disclose a method 5 of recording a time that the sensors output indicates an existence of a power consumption property at a predetermined value.

Boutaghou teaches a method of controlling the temperature of components that can reach and exceed desirable temperatures wherein if the temperature exceeds a 10 certain threshold an appropriate action is executed to address the temperature.

Boutaghou discloses monitoring the individual components wherein when one of the components exceed a maximum temperature the amount of time that component has exceeded the max temperature is recorded as P [Col 7 lines 19-26].

15 It would have been obvious to one of ordinary skill in the art to combine the teachings of Rotem and Boutaghou because they both teach methods of compensating for high temperatures by taking appropriate action due to excess temperature readings.

One of ordinary skill in the art would be motivated to make this combination of including the ability to record the amount of time an excess temperature exist as taught by

20 Boutaghou, as doing so would give the added benefit of power conservation and further prevention of damaging the chip due to excessive temperatures for extended periods of time.

As per claims 2, 10, and 15, Rotem in view of Boutaghou teach the invention wherein the power consumption property of the chip comprises temperature, and the temperature comprises a temperature range including one or more temperatures [Col 7 lines 19-26; wherein if it is measured whether the temperature still exceeds a maximum 5 temperature during a certain time period it would have been obvious of ordinary skill in the art to measure the temperature at different time intervals with a result of more than one temperature reading thus a range].

As per claims 3, 11, and 16, Rotem in view of Boutaghou teach the invention 10 wherein each sensor output corresponds to a temperature range, and indicates the existence of the one or more temperatures measured at the corresponding sensor output [Col 7 lines 19-26; wherein if it is measured whether the temperature still exceeds a maximum temperature during a certain time period it would have been obvious of ordinary skill in the art to measure the temperature at different time intervals 15 with a result of more than one temperature reading thus a range].

As per claims 4, 12 and 17, Rotem in view of Boutaghou teach the invention wherein the power consumption property of the chip comprises voltage drop, and wherein the voltage drop range includes one or more voltage drops [wherein it would 20 have been obvious to one of ordinary skill in the art to include a voltage drop as the power consumption property of the chip because power consumption and temperature

Art Unit: 2115

are related and directly proportionate when dealing with the art of chips [Page 1, paragraph 0007]].

As per claims 5, 13, and 18, Rotem in view of Boutaghou teach the invention

5 wherein each sensor output corresponds to a voltage drop range, and each sensor output indicates the existence of a voltage drop measured at the corresponding output [wherein it would have been obvious to one of ordinary skill in the art to include a voltage drop as the power consumption property of the chip because power consumption and temperature are related and directly proportionate when dealing with

10 the art of chips [Page 1, paragraph 0007]].

As per claims 6-8, it is directed to the method of steps to implement the system as set forth in claims 14-18. Therefore, it is rejected for the same basis as set forth hereinabove.

15

As per claims 9-13, it is directed to an apparatus to implement the system as set forth in claims 14-18. Therefore, it is rejected for the same basis as set forth hereinabove.

20 **As per claims 19-23,** it is directed to a machine-readable medium to implement the method of steps as set forth in claims 14-18. Therefore, it is rejected for the same basis as set forth hereinabove.

Art Unit: 2115

Conclusion

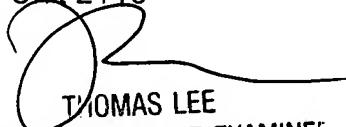
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Malcolm D. Cribbs whose telephone number is 571-272-5689. The examiner can normally be reached on M-F 8AM-430PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

20 September 4, 2007

Malcolm D Cribbs
Examiner
Art Unit 2115



THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100